Formation of Metal-Semiconductor Axial Nanowire Heterostructures through Controlled Silicidation

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Abstract

Semiconductor nanowires show promise for application in nanoscale electronics, but the difficulty of forming low-resistance ohmic contacts provides a challenge to their implementation. To improve the electrical performance of lithographically defined nickel contacts, nickel-silicide/silicon axial nanowire heterostructures were formed by controlled partial silicidation. Prior to annealing, two-terminal silicon nanowire devices had nonlinear and asymmetric current-voltage behavior indicative of poor electrical contacts. After the formation of heterostructure contacts, nanowire devices carried increased current, pointing to reduced contact resistance, and a larger fraction of nanowire devices exhibited linear current-voltage characteristics. A study of the silicidation kinetics revealed a linear growth rate of 0.2 μm/min, suggesting the rate may be limited by the silicidation reaction at the interface.

Introduction

Semiconductor nanowires are one class of building blocks that show promise for application in digital electronics and computing within a bottom-up paradigm for nanotechnology.[1,2] One challenge to their implementation is the reliable formation of low-resistance ohmic electrical contacts. Metal-semiconductor axial nanowire heterostructures, formed both during growth[3] and by postsynthesis processing,[4–10] often have atomically abrupt coherent interfaces and therefore can be ideal electrical contacts.[6,7] Since they are much smaller than lithographically defined contacts, axial heterostructure contacts also reduce gate voltage screening in nanowire field effect transistors (FETs).[8] Of particular interest are nickel-silicide/silicon (Ni_xSi_y-Si) axial nanowire heterostructures that recently have been used as nanowire contacts.[4–7] They are usually formed by a rapid thermal anneal in which nickel diffuses from the lithographically defined contact into the Si nanowire and converts a section of it into Ni_xSi_y (Figure 1a). This controlled silicidation can be used to define FET channel lengths smaller than those defined with lithographic techniques.[7,8]

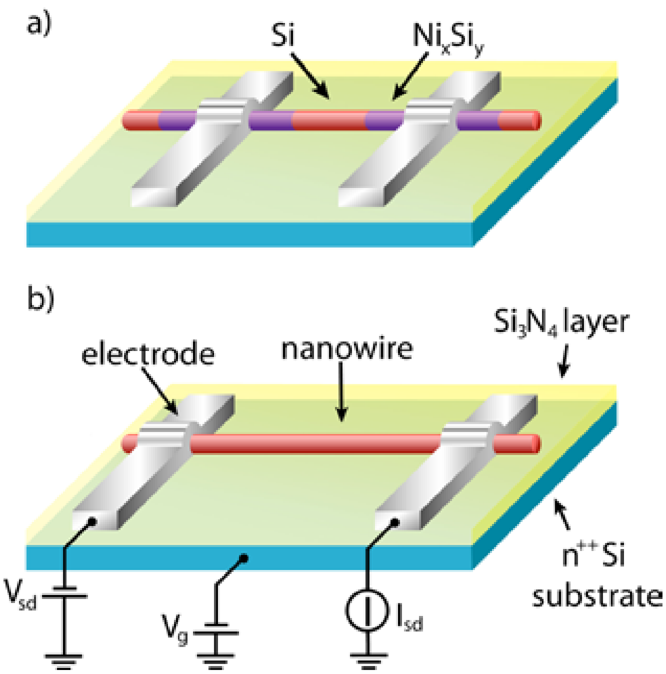

Figure 1. (a) Schematic of a Si nanowire (red), Ni electrodes (silver), and Ni_xSi_y segments (purple). (b) Schematic of a nanowire field effect transistor. Source-drain voltage, gate voltage, and source-drain current are V_{sd}, V_g, and I_{sd}, respectively.

Such efforts are informed by the large amount of work done by the semiconductor industry in developing silicides for commercial application.[11] A related study analyzed the diameter dependence of nanowire silicidation and showed that diffusion takes place through the core of the wire as opposed to the surface.[5,7] However, the characterization of nanowire silicidation and its effects on FET electrical behavior is not complete. Successful development of metal-semiconductor axial heterostructures as low-resistance electrical contacts will allow the nanowire and junction properties to determine FET device performance in a controlled manner. This paper reports advances in characterization of Ni_xSi_y-Si axial nanowire heterostructure formation and application in FETs, including a study of silicidation kinetics and electrical contact behavior. Scanning electron and optical microscopy were employed in conjunction with two-terminal electrical transport measurements.

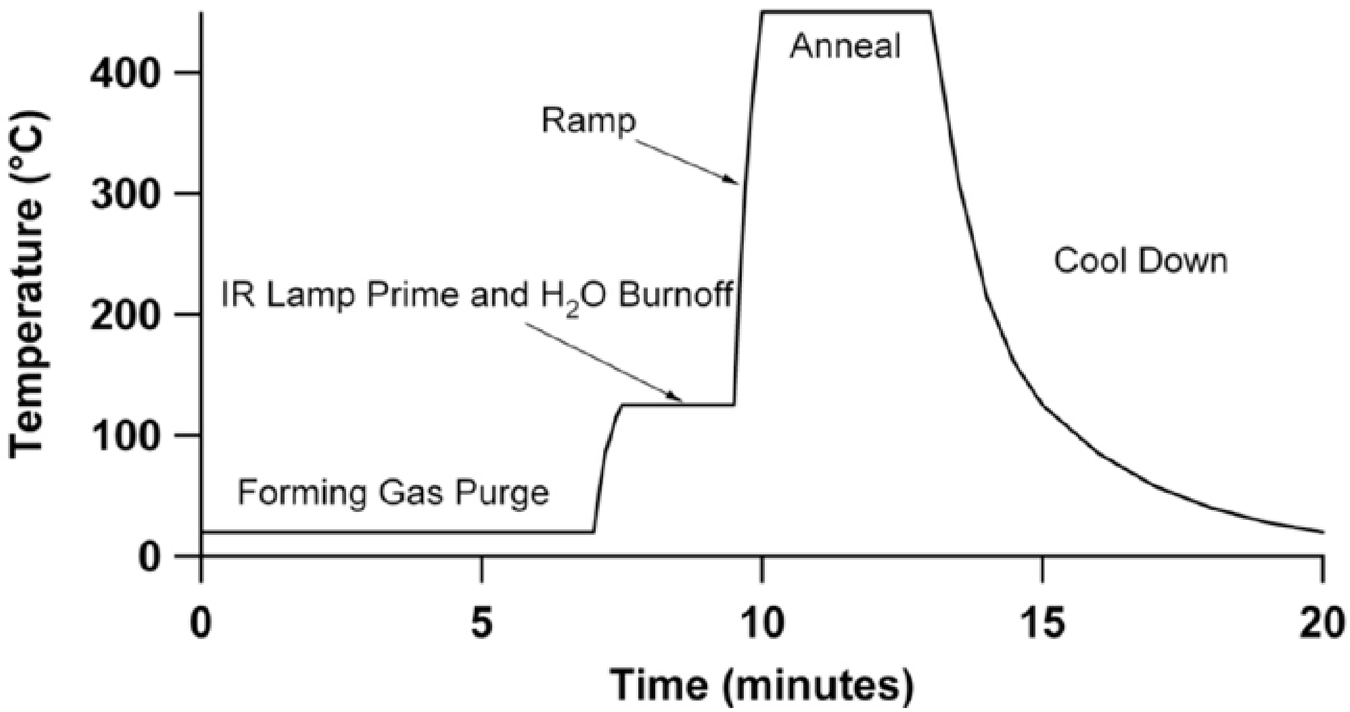

Figure 2. Temperature as a function of time during a rapid thermal anneal. In this example, the sample spends 3 min at the 450° C annealing temperature. The process quickly ramps to the anneal temperature in order to minimize the time spent at intermediate temperatures.

Background

Nanowires

Semiconductor nanowires are typically single crystal and are nanometers in diameter and microns in length. They are most often grown through the metal-catalyzed vapor-liquid-solid mechanism combined with a chemical vapor deposition process.[12] The catalyst at the tip of the nanowire, often gold, controls diameter, and the time of growth controls the length.[13] Nanowire composition can be controlled by selection of gas-phase reactants, including the addition of dopants. Radial and axial heterostructures can be formed by changing growth temperature or gas-phase reactants during growth.[14,15] Temperature, pressure, flow rate, and atmosphere can affect the growth rate, crystal growth direction, and morphology. As size, composition, morphology, and structure affect the properties of the nanowire, control over growth can allow properties to be tailored for a specific application. Nanowires are being investigated for application in chemical/biological sensing and detection, digital electronics and computing, photonics, and future nanosystems. Such applications require nanowires to be assembled into arrays and have been demonstrated using dielectrophoretic forces.[16]

Field Effect Transistors

FETs are the most prolific component of all digital electronics since they are able to act as both a switch and an amplifier. A nanowire can be used as an FET that operates similarly to those fabricated in the semiconductor industry (Figure 1b). The two contact electrodes, known as the source and the drain, define the length of the nanowire FET channel. The conductive substrate acts as a common back-gate electrode, since it is coated by an insulating film. Its operation is similar to that of a capacitor; applying a gate voltage allows the conductivity of the nanowire channel to be modulated.[17] However, in order for the FET function to be dominated by the nanowire properties, the source and drain electrodes must be low-resistance ohmic electrical contacts.

Silicidation

Silicidation is a process in which metal and Si are in contact at high temperature, and their atoms interdiffuse to form a metal silicide. These are intermetallic stoichiometric compounds, M_xSi_y, that typically have metallic behavior. The semiconductor industry uses silicides as contact materials, since they can form low-resistance contacts and often have other desirable properties such as high thermal stability.[11] Appropriate metal selection, deposition, and careful processing are essential to the formation of an atomically abrupt interface between the crystalline silicon and silicide, since buckling may occur if they are not lattice matched[9] or the silicidation is not well controlled. Here, nickel silicides are of interest where Ni diffuses interstitially in Si.[18] However, once nickel silicide forms, the Ni must diffuse through the Ni_xSi_y where its diffusion is slower.[7] The three most common phases, in order of increasing formation temperature, are Ni_2Si, NiSi, and $NiSi_2$.[19,20] The NiSi-Si system is particularly favorable for the formation of atomically abrupt interfaces because NiSi and Si have comparable lattice constants and atomic densities.[6,7] NiSi forms a Schottky contact with silicon, but with doping the barrier narrows so that carriers can tunnel through it, producing an ohmic contact to both p- and n-type Si.[19] The barrier may be further narrowed by segregation of dopants to the Ni_xSi_y–Si interface during silicidation.[19]

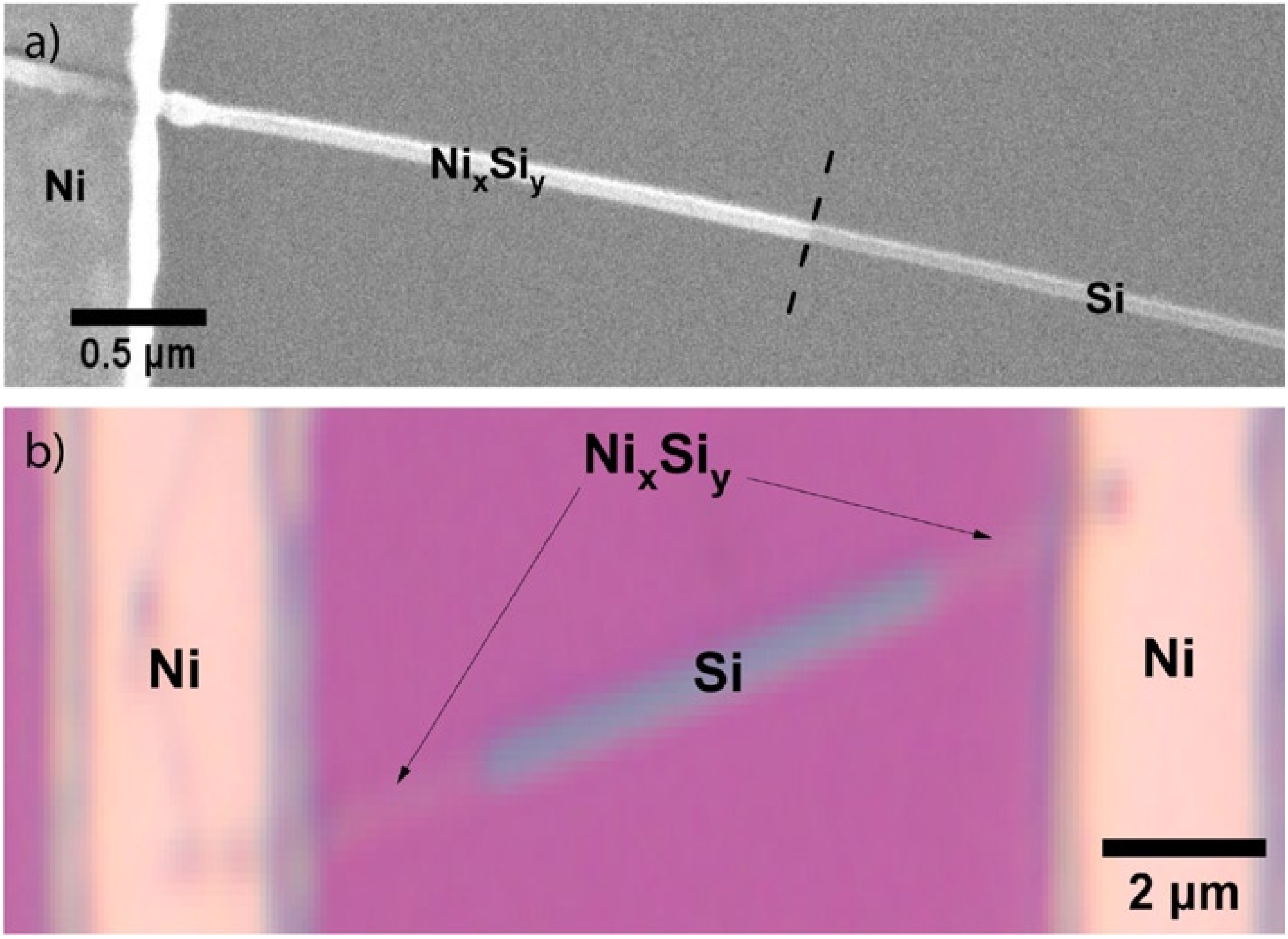

Figure 3. (a) A scanning electron microscope image of a silicon nanowire contacted lithographically with Ni and then annealed to form a Ni_xSi_y-Si heterostructure. The dotted line is a guide to the eyes. (b) An optical microscope image of a Si nanowire implemented as a field effect transistor with Ni_xSi_y-Si heterostructures as contacts.

Approach

In order to form metal-semiconductor heterostructures, nanowires are transferred to a device substrate, contacted by metal, and annealed at high temperature. The nanowires used in this study were 50 nm diameter p-type Si, and the device substrates were n^{++}-Si with a 200 nm thin film coating of Si_3N_4. Due to their small size, individual nanowires cannot be mechanically transferred from the growth substrate to the device substrate. Nanowires were therefore sonicated in ethanol and subsequently drop-cast on substrates. A contact pattern was defined using photolithography, which was chosen over electron beam lithography because it is fast and economical. To prepare for metal evaporation, the substrate was treated with an oxygen plasma to remove resist residue and dipped in hydrofluoric acid to remove the native oxide on the Si nanowires. This process allowed contact to be made directly to the Si. Ni was evaporated using an electron-beam metal evaporation system. This technique was preferred over sputtering or electrodeposition because it uses high vacuum levels, which prevent oxidation, and high purity source metals to reduce introduction of impurities. After nanowires were contacted with Ni, the Ni_xSi_y-Si heterostructures were formed by silicidation during a rapid thermal anneal (RTA) at 450° C for 1–5 min. The fast temperature ramp time (~30 sec) of the RTA reduces the amount of time spent at intermediate temperatures. During RTA, Ni atoms diffuse from the lithographically defined contact into the Si nanowire and convert it into Ni_xSi_y. The temperature as a function of time for a typical anneal is shown in Figure 2. Scanning electron microscopy (SEM) was used to verify the formation of Ni_xSi_y. In order to study the silicidation kinetics, SEM was also used to measure the length of the Ni_xSi_y. As a faster and economical alternative, optical microscopy (OM) was also employed for measurements. Two-terminal electrical transport measurements were also conducted before and after annealing in order to observe the change in electrical behavior of the nanowire devices.

Results and Discussion

Ni_xSi_y-Si nanowire heterostructures were successfully formed, as evidenced by SEM, OM, and electrical transport measurements. An abrupt change in signal intensity along the nanowire, indicating a transition between Ni_xSi_y and Si, was observed, as shown in a typical

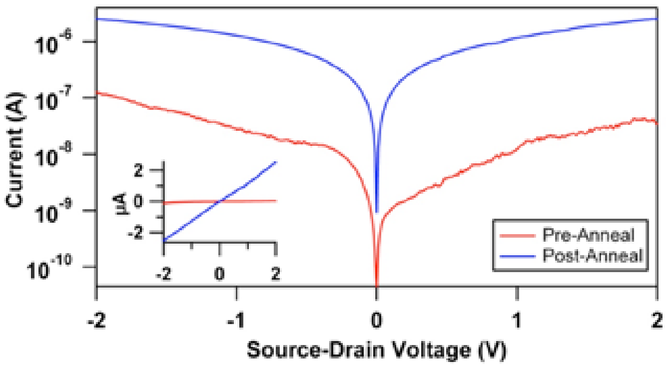

Figure 4. A semi-log plot of current as a function of source-drain voltage for a representative silicon nanowire FET. The pre- and post-anneal curves are shown in red and blue, respectively. After annealing, the contact resistance decreases and the behavior becomes ohmic. The inset shows the linearly scaled plot.

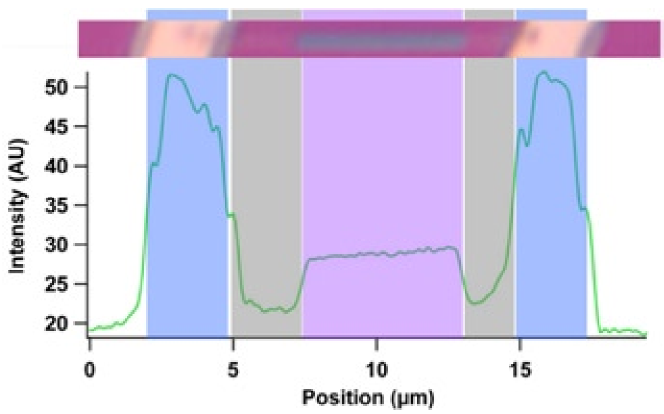

Figure 5. A profile of green reflected intensity along the longitudinal axis of the nanowire and its contacts. The data are from the red-green-blue optical microscope image that is aligned above. The Ni contacts, Ni_xSi_y, and Si channel are indicated by the blue, gray, and purple shaded regions, respectively.

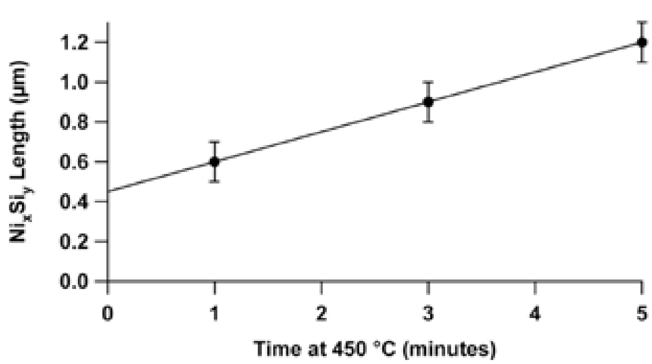

Figure 6. Ni_xSi_y length as a function of time at 450° C.

post-anneal SEM image (Figure 3a) and OM image (Figure 3b). Silicidation reduced the 5 to 10 μm channel length of the nanowire FET by about 1 μm, depending on anneal time. Although phase was not determined in this study, thin-film literature shows that NiSi will form at 450° C.[19] Further evidence of heterostructure formation is shown by pre- and post-anneal current-voltage (I-V) behavior for a representative nanowire device (Figure 4). After annealing the current carried at 2 V increased by over an order of magnitude. Since the silicidation temperature was the same as the growth temperature, the silicidation anneal is not expected to have a measurable impact on the conductivity of the nanowires themselves. High-resolution transmission electron microscopy also shows that the majority of nanowires are defect free, and thus the increased current is not attributed to a reduction of defects. An increased current cannot be fully accounted for by the observed reduction in channel length and suggests that the contact resistance was greatly reduced. Furthermore, the pre-anneal I-V behavior is asymmetric, which is indicative of a poor contact. It becomes linear after annealing, again indicating improved electrical contact. Such changes in electrical behavior can be attributed to the differences between the lithographically defined polycrystalline Ni and the Ni_xSi_y. From reported high-resolution transmission electron microscopy, it is expected that the formed Ni_xSi_y is a single crystal and that the heterostructure contact interface is epitaxial, coherent, and atomically abrupt.[6,7] This is in stark contrast to the interface between a polycrystalline metal and single-crytal silicon, where grain size affects surface wetting and more surface states may exist. The contact geometry also changes as the lithographic contact blankets the nanowire surface while the heterostructure contact is defined by the cross-section of the nanowire.

The optical microscopy studies also enabled a quantitative study of the silicidation kinetics. The length of the Ni_xSi_y was measured by taking an intensity profile along the longitudinal axis of the nanowire in the red-green-blue OM image. Interfaces between different regions were defined by the midpoint in green intensity between the regions (Figure 5). The OM measurement technique had an unexpectedly high resolution of ± 0.1 μm, as verified by SEM. This resolution is attributed to the accuracy associated with the measurement of a single midpoint of intensity, rather than the resolution of two distinct objects. This resolution was sometimes compromised by features of the sample that might interfere with the measurement, including poorly defined contact edges and debris. A linear relationship between silicide length and time spent at the 450° C annealing temperature was observed (Figure 6). The best linear fit of the data resulted in a growth rate of 0.2 μm/min and a y-intercept of 0.5 μm. In establishing the linear relationship, a time zero point was not used, due to the error caused by finite time spent between the anneal temperature and the lowest temperature at which silicidation occurs. Prior to annealing there is no silicidation, but silicidation has been reported to occur at temperatures as low as 200° C.[21] Accounting for such error quantitatively is difficult, as the rate-limiting step is likely to be temperature dependent.

The silicide growth could be limited by the supply of Ni, the diffusion of Ni through the Ni_xSi_y, or the silicidation reaction at the Ni_xSi_y-Si interface. Since the lithographic Ni contacts are large in comparison with the Si nanowire, the supply of Ni is not expected to be rate limiting. Ni diffusion could limit the growth because, as the Ni_xSi_y section lengthens, the Ni atoms need to diffuse further. The growth rate does not decrease with time, however, ruling out this possibility. Instead, the constant growth rate indicates that the growth is limited by the silicidation reaction at the Ni_xSi_y-Si interface. Linear growth of NiSi was reported for silicidation of Si nanowires crossed by Ni nanowires at anneal temperatures from 500° to 650° C, with rates of 0.3 and 6.7 nm/min, respectively.[7] However, this system is different from that used in this study, as the crossed nanowires are 20 nm in diameter and have a point contact interface, which may result in silicidation limited by the dissolution of Ni through the point contact.[7] Future studies could provide further evidence that the growth is indeed limited by the silicidation reaction at the growth interface.

Conclusion

Ni_xSi_y-Si axial nanowire heterostructures were successfully formed by partial silicidation and implemented as contacts for nanowire FETs. After the formation of heterostructure contacts, nanowire FETs carried increased current, suggesting reduced contact resistance, and showed improved ohmic behavior. These results are attributed to the differences between the lithographically defined nickel contacts and the Ni_xSi_y heterostructure contacts. SEM and OM were used to investigate the silicidation, and kinetics and OM were shown to have an unexpectedly high resolution of ± 0.1 μm. A linear growth rate of 0.2 μm/min was observed and may indicate that the growth is limited by the silicidation reaction at the Ni_xSi_y-Si interface. The reduced contact resistance, combined with improved current-voltage behavior and controllable silicidation, makes such metal-semiconductor heterostructures a promising option for making reliable electrical contact to semiconductor nanowires.

Both future SEM studies of silicidation at short time scales and determination of the growth activation energy could provide further confirmation that the growth rate is limited by the silicidation reaction at the interface at higher temperatures. Also, the phase of Ni_xSi_y in the formed heterostructure could be determined by electron backscatter diffraction. Effects of varying other experimental parameters, including temperature, atmosphere, and metal thickness, should be further investigated. Development of such a heterostructure could also be extended to other potentially useful systems, including germanium nanowires.

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